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Search Results -

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(5 AND 2).PGPB,USPT.	40
(L5 AND L2).PGPB,USPT.	40

Database:
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US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Monday, May 17, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT; PLUR=YES; OP=OR		
L6	L5 and l2	40	L6
L5	L4 or l3	4088	L5
L4	(717/101-108)![CCLS]	891	L4
L3	(712/10-36)![CCLS]	3201	L3
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L2	(host or server) near10 (instal$4 or download$3 or transfer$5 or sent or send$3 or stor$3 or sav$3) and compil$6 near6 (source or code or program) and (second$5 or plural$5 or multiple or auxil$6 or assist$3) near6 (slav$3 or co near2 process$3 or dsp)	237	L2
L1	(host or server) near10 (instal$4 or download$3 or transfer$5 or sent or send$3 or stor$3 or sav$3) and compil$6 and (second$5 or plural$5 or multiple or auxil$6 or assist$3) near6 (slav$3 or co near2 process$3 or dsp)	445	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6738837 B1

Using default format because multiple data bases are involved.

L3: Entry 1 of 4 File: USPT May 18, 2004

US-PAT-NO: 6738837
DOCUMENT-IDENTIFIER: US 6738837 B1

TITLE: Digital system with split transaction memory access

DATE-ISSUED: May 18, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wyland; David C.	Morgan Hill	CA		

US-CL-CURRENT: 710/25; 710/15, 710/22, 710/23, 710/24, 710/26, 710/27, 710/28, 712/22

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☑ 2. Document ID: US 6678817 B1

L3: Entry 2 of 4 File: USPT Jan 13, 2004

US-PAT-NO: 6678817
DOCUMENT-IDENTIFIER: US 6678817 B1

TITLE: Method and apparatus for fetching instructions from the memory subsystem of a mixed architecture processor into a hardware emulation engine

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 3. Document ID: US 6289441 B1

L3: Entry 3 of 4 File: USPT Sep 11, 2001

US-PAT-NO: 6289441
DOCUMENT-IDENTIFIER: US 6289441 B1

TITLE: Method and apparatus for performing multiple branch predictions per cycle

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 4. Document ID: US 5802346 A

L3: Entry 4 of 4 File: USPT Sep 1, 1998

US-PAT-NO: 5802346
DOCUMENT-IDENTIFIER: US 5802346 A

TITLE: Method and system for minimizing the delay in executing branch-on-register instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
CLOCK	538329
CLOCKS	75234
CYCLE	1069115
CYCLES	429109
SENT	700502
SENTS	16641
STALL$3	0
STALL	35705
STALLA	264
STALLABL	1
STALLAD	3
((CLOCK OR CYCLE) NEAR7 (STALL$3 OR SUSPEND$3) NEAR10 ADDRESS$3 NEAR7 (FETCH$3 OR SEND$3 OR SENT) AND PIPELIN$6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	4

There are more results than shown above. Click here to view the entire set.

Display Format: - Change Format

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h e b b g e e e f e ef b e

Refine Search

Search Results -

Term	Documents
ONE	10481841
ONES	508855
SINGLE	3211843
SINGLES	3037
INTEGRATED	1042935
INTEGRATEDS	3
CHIP	538354
CHIPS	245031
CONTEXT	267777
CONTEXTS	21279
SWITCH$3	0
((ONE OR SINGLE) NEAR5 (INTEGRATED OR CHIP) NEAR9 CONTEXT NEAR2 SWITCH$3 NEAR9 MICROPROCESSOR$1).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	3

There are more results than shown above. Click here to view the entire set.

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, May 20, 2004 Printable Copy Create Case

Set Name side by	Query	Hit Count	Set Name result set

h e b b cg b e e ch

side

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L1	(one or single) near5 (integrated or chip) near9 context near2 switch$3 near9 microprocessor$1	3	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Hit List

Your wildcard search against 10000 terms has yielded the results below.
Your result set for the last L# is incomplete.
The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 21 through 36 of 36 returned.

☐ 21. Document ID: US 5777629 A

Using default format because multiple data bases are involved.

L9: Entry 21 of 36 File: USPT Jul 7, 1998

US-PAT-NO: 5777629
DOCUMENT-IDENTIFIER: US 5777629 A

TITLE: Graphics subsystem with smart direct-memory-access operation

DATE-ISSUED: July 7, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Baldwin; David Robert	Weybridge			GB

US-CL-CURRENT: 345/506; 345/505, 345/519

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 22. Document ID: US 5758113 A

L9: Entry 22 of 36 File: USPT May 26, 1998

US-PAT-NO: 5758113
DOCUMENT-IDENTIFIER: US 5758113 A

TITLE: Refresh control for dynamic memory in multiple processor system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 23. Document ID: US 5694150 A

L9: Entry 23 of 36 File: USPT Dec 2, 1997

US-PAT-NO: 5694150

h e b b cg b cc e

DOCUMENT-IDENTIFIER: US 5694150 A

TITLE: Multiuser/multi pointing device graphical user interface system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 24. Document ID: US 5594903 A

L9: Entry 24 of 36 File: USPT Jan 14, 1997

US-PAT-NO: 5594903
DOCUMENT-IDENTIFIER: US 5594903 A

TITLE: Operating System architecture with reserved memory space resident program code identified in file system name space

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 25. Document ID: US 5588111 A

L9: Entry 25 of 36 File: USPT Dec 24, 1996

US-PAT-NO: 5588111
DOCUMENT-IDENTIFIER: US 5588111 A

TITLE: Fault-tolerant computer system having switchable I/O bus interface modules

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 26. Document ID: US 5572666 A

L9: Entry 26 of 36 File: USPT Nov 5, 1996

US-PAT-NO: 5572666
DOCUMENT-IDENTIFIER: US 5572666 A
**** See image for Certificate of Correction ****

TITLE: System and method for generating pseudo-random instructions for design verification

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 27. Document ID: US 5388242 A

L9: Entry 27 of 36 File: USPT Feb 7, 1995

US-PAT-NO: 5388242
DOCUMENT-IDENTIFIER: US 5388242 A

TITLE: Multiprocessor system with each processor executing the same instruction

h e b b cg b cc e

sequence and hierarchical memory providing on demand page swapping

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 28. Document ID: US 5384906 A

L9: Entry 28 of 36 File: USPT Jan 24, 1995

US-PAT-NO: 5384906
DOCUMENT-IDENTIFIER: US 5384906 A

TITLE: Method and apparatus for synchronizing a plurality of processors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 29. Document ID: US 5327553 A

L9: Entry 29 of 36 File: USPT Jul 5, 1994

US-PAT-NO: 5327553
DOCUMENT-IDENTIFIER: US 5327553 A

TITLE: Fault-tolerant computer system with /CONFIG filesystem

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 30. Document ID: US 5317752 A

L9: Entry 30 of 36 File: USPT May 31, 1994

US-PAT-NO: 5317752
DOCUMENT-IDENTIFIER: US 5317752 A

TITLE: Fault-tolerant computer system with auto-restart after power-fall

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 31. Document ID: US 5317726 A

L9: Entry 31 of 36 File: USPT May 31, 1994

US-PAT-NO: 5317726
DOCUMENT-IDENTIFIER: US 5317726 A

TITLE: Multiple-processor computer system with asynchronous execution of identical code streams

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

h e b b cg b cc e

☐ 32. Document ID: US 5295258 A

L9: Entry 32 of 36 File: USPT Mar 15, 1994

US-PAT-NO: 5295258
DOCUMENT-IDENTIFIER: US 5295258 A

TITLE: Fault-tolerant computer system with online recovery and reintegration of redundant components

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 33. Document ID: US 5276823 A

L9: Entry 33 of 36 File: USPT Jan 4, 1994

US-PAT-NO: 5276823
DOCUMENT-IDENTIFIER: US 5276823 A

TITLE: Fault-tolerant computer system with redesignation of peripheral processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 34. Document ID: US 5193175 A

L9: Entry 34 of 36 File: USPT Mar 9, 1993

US-PAT-NO: 5193175
DOCUMENT-IDENTIFIER: US 5193175 A

TITLE: Fault-tolerant computer with three independently clocked processors asynchronously executing identical code that are synchronized upon each voted access to two memory modules

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 35. Document ID: US 5146589 A

L9: Entry 35 of 36 File: USPT Sep 8, 1992

US-PAT-NO: 5146589
DOCUMENT-IDENTIFIER: US 5146589 A

TITLE: Refresh control for dynamic memory in multiple processor system

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 36. Document ID: US 4965717 A

h e b b cg b cc e

L9: Entry 36 of 36 File: USPT Oct 23, 1990

US-PAT-NO: 4965717
DOCUMENT-IDENTIFIER: US 4965717 A
** See image for Reexamination Certificate **

TITLE: Multiple processor system having shared memory with private-write capability

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
CONTEXT	267777
CONTEXTS	21279
SWITCH$12	0
SWITCH	1813455
SWITCHA	210
SWITCHAABLE	1
SWITCHAAID	1
SWITCHAAP	1
SWITCHAB	11
SWITCHABAR	1
SWITCHABE	5
(L8 AND CONTEXT NEAR1 SWITCH$12).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	36

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Search Results - Record(s) 1 through 20 of 23 returned.

☐ 1. Document ID: US 20040039901 A1

Using default format because multiple data bases are involved.

L22: Entry 1 of 23 File: PGPB Feb 26, 2004

PGPUB-DOCUMENT-NUMBER: 20040039901
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040039901 A1

TITLE: Data processing device and electronic equipment

PUBLICATION-DATE: February 26, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kudo, Makoto	Nagano-ken		JP	

US-CL-CURRENT: 712/237; 712/205

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 20040039897 A1

L22: Entry 2 of 23 File: PGPB Feb 26, 2004

PGPUB-DOCUMENT-NUMBER: 20040039897
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040039897 A1

TITLE: Data processing device and electronic equipment

PUBLICATION-DATE: February 26, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kudo, Makoto	Nagano-ken		JP	

US-CL-CURRENT: 712/213; 712/209

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e b ef b e

☐ 3. Document ID: US 20030037228 A1

L22: Entry 3 of 23 File: PGPB Feb 20, 2003

PGPUB-DOCUMENT-NUMBER: 20030037228
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030037228 A1

TITLE: System and method for instruction level multithreading scheduling in a embedded processor

PUBLICATION-DATE: February 20, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kelsey, Nicholas J.			US	
Waters, Christopher J. F.			US	
Mimaroglu, Tibet			US	
Fotland, David A.			US	

US-CL-CURRENT: 712/245

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 20020184472 A1

L22: Entry 4 of 23 File: PGPB Dec 5, 2002

PGPUB-DOCUMENT-NUMBER: 20020184472
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020184472 A1

TITLE: Microcomputer

PUBLICATION-DATE: December 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Ohsuga, Hiroshi	Tokyo		JP	
Kiuchi, Atsushi	Tokyo		JP	
Hasegawa, HIronobu	Tokyo		JP	
Baji, Toru	Tokyo		JP	
Noguchi, Koki	Tokyo		JP	
Akao, Yasushi	Tokyo		JP	
Baba, Shiro	Tokyo		JP	

US-CL-CURRENT: 712/33; 712/35

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e b ef b e

☐ 5. Document ID: US 20020144100 A1

L22: Entry 5 of 23 File: PGPB Oct 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020144100
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020144100 A1

TITLE: Peak power reduction when updating future file

PUBLICATION-DATE: October 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Inoue, Ryo	Austin	TX	US	
Revilla, Juan G.	Austin	TX	US	

US-CL-CURRENT: 712/228

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 6. Document ID: US 20020144093 A1

L22: Entry 6 of 23 File: PGPB Oct 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020144093
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020144093 A1

TITLE: Method and apparatus for restoring registers after cancelling a multi-cycle instruction

PUBLICATION-DATE: October 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Inoue, Ryo	Austin	TX	US	
Overkamp, Gregory A.	Austin	TX	US	

US-CL-CURRENT: 712/218

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 7. Document ID: US 20020144089 A1

L22: Entry 7 of 23 File: PGPB Oct 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020144089
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020144089 A1

h e b b g e e e f e b ef b e

TITLE: Use of a future file for data address calculations in a pipelined processor

PUBLICATION-DATE: October 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Anderson, William C.	Austin	TX	US	
Inoue, Ryo	Austin	TX	US	

US-CL-CURRENT: 712/216

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 8. Document ID: US 20020091916 A1

L22: Entry 8 of 23 File: PGPB Jul 11, 2002

PGPUB-DOCUMENT-NUMBER: 20020091916
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020091916 A1

TITLE: Embedded-DRAM-DSP architecture

PUBLICATION-DATE: July 11, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dowling, Eric M.	Richardson	TX	US	

US-CL-CURRENT: 712/228; 712/32

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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☐ 9. Document ID: US 20020087845 A1

L22: Entry 9 of 23 File: PGPB Jul 4, 2002

PGPUB-DOCUMENT-NUMBER: 20020087845
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020087845 A1

TITLE: Embedded-DRAM-DSP architecture

PUBLICATION-DATE: July 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dowling, Eric M.	Richardson	TX	US	

US-CL-CURRENT: 712/228; 712/32

h e b b g e e e f e b ef b e

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 10. Document ID: US 20020078333 A1

L22: Entry 10 of 23 File: PGPB Jun 20, 2002

PGPUB-DOCUMENT-NUMBER: 20020078333
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020078333 A1

TITLE: Resource efficient hardware loops

PUBLICATION-DATE: June 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Inoue, Ryo	Austin	TX	US	
Singh, Ravi P.	Austin	TX	US	
Roth, Charles P.	Austin	TX	US	
Overkamp, Gregory A.	Austin	TX	US	

US-CL-CURRENT: 712/241

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 11. Document ID: US 20020078326 A1

L22: Entry 11 of 23 File: PGPB Jun 20, 2002

PGPUB-DOCUMENT-NUMBER: 20020078326
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020078326 A1

TITLE: Speculative register adjustment

PUBLICATION-DATE: June 20, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Roth, Charles P.	Austin	TX	US	
Singh, Ravi P.	Austin	TX	US	
Overkamp, Gregory A.	Austin	TX	US	

US-CL-CURRENT: 712/218; 712/227, 712/235, 712/241

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e b ef b e

☐ 12. Document ID: US 20020040429 A1

L22: Entry 12 of 23 File: PGPB Apr 4, 2002

PGPUB-DOCUMENT-NUMBER: 20020040429
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020040429 A1

TITLE: Embedded-DRAM-DSP architecture

PUBLICATION-DATE: April 4, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Dowling, Eric M.	Richardson	TX	US	

US-CL-CURRENT: 712/228

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 13. Document ID: US 20020038416 A1

L22: Entry 13 of 23 File: PGPB Mar 28, 2002

PGPUB-DOCUMENT-NUMBER: 20020038416
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020038416 A1

TITLE: System and method for reading and writing a thread state in a multithreaded central processing unit

PUBLICATION-DATE: March 28, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Fotland, David A.	San Jose	CA	US	
Mimaroglu, Tibet	Sunnyvale	CA	US	

US-CL-CURRENT: 712/228

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 14. Document ID: US 20020002667 A1

L22: Entry 14 of 23 File: PGPB Jan 3, 2002

PGPUB-DOCUMENT-NUMBER: 20020002667
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020002667 A1

TITLE: System and method for instruction level multithreading in an embedded

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processor using zero-time context switching

PUBLICATION-DATE: January 3, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kelsey, Nicholas J.	Mountain View	CA	US	
Waters, Christopher J.	Palo Alto	CA	US	
Mimaroglu, Tibet	Sunnyvale	CA	US	
Fotland, David A.	San Jose	CA	US	

US-CL-CURRENT: 712/228

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 15. Document ID: US 6567895 B2

L22: Entry 15 of 23 File: USPT May 20, 2003

US-PAT-NO: 6567895
DOCUMENT-IDENTIFIER: US 6567895 B2

TITLE: Loop cache memory and cache controller for pipelined microprocessors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 16. Document ID: US 6434690 B1

L22: Entry 16 of 23 File: USPT Aug 13, 2002

US-PAT-NO: 6434690
DOCUMENT-IDENTIFIER: US 6434690 B1
**** See image for Certificate of Correction ****

TITLE: Microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CUP-type instructions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 17. Document ID: US 6405302 B1

L22: Entry 17 of 23 File: USPT Jun 11, 2002

US-PAT-NO: 6405302
DOCUMENT-IDENTIFIER: US 6405302 B1

TITLE: Microcomputer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b g e e e f e b ef b e

☐ 18. Document ID: US 6260136 B1

L22: Entry 18 of 23 File: USPT Jul 10, 2001

US-PAT-NO: 6260136
DOCUMENT-IDENTIFIER: US 6260136 B1

TITLE: Substitute register for use in a high speed data processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 19. Document ID: US 5867726 A

L22: Entry 19 of 23 File: USPT Feb 2, 1999

US-PAT-NO: 5867726
DOCUMENT-IDENTIFIER: US 5867726 A

TITLE: Microcomputer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 20. Document ID: US 5794062 A

L22: Entry 20 of 23 File: USPT Aug 11, 1998

US-PAT-NO: 5794062
DOCUMENT-IDENTIFIER: US 5794062 A

TITLE: System and method for dynamically reconfigurable computing using a processing unit having changeable internal hardware organization

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
(18 AND 21).PGPB,USPT.	23
(L21 AND L18).PGPB,USPT.	23

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L9	L8 and l4	82	L9
L8	(halt$3 or inhibit$3 or suspend$3 or suspension$1 hold$3 or held) near6 pipelin$6	3325	L8
L7	(712/23-219)![CCLS]	5589	L7
L6	(711/147-153)[CCLS]	2403	L6
L5	L4 and microprocessor$1 and communication$1	343	L5
L4	l1 or L3	1248	L4
L3	(712/227-229)![CCLS]	1070	L3
L2	(718/108)![CCLS]	250	L2
L1	(718/108)[CCLS]	250	L1

END OF SEARCH HISTORY

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Refine Search

Search Results -

Term	Documents
SUSPENSION	350104
SUSPENSIONS	126949
SUSPEND$3	0
SUSPEND	42296
SUSPENDA	1
SUSPENDACK	2
SUSPENDALY	1
SUSPENDANT	28
SUSPENDATE	2
SUSPENDBP	1
SUSPENDCD	1
(L20 AND (SUSPEND$3 OR SUSPENSION)).PGPB,USPT.	15

There are more results than shown above. Click here to view the entire set.

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L21

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Tuesday, May 18, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=PGPB,USPT; PLUR=YES; OP=OR		

h e b b cg b e e ch

L21	L20 and (suspend$3 or suspension)	15	L21
L20	L19 and l16	24	L20
L19	(plur$7 or multiple or second) near5 pipelin$6 and L14	39	L19
L18	L17 and l15	58	L18
L17	(712/2-300)[CCLS]	9790	L17
L16	(712/2-300)![CCLS]	9790	L16
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L15	(plur$7 or multiple or second) and L14	116	L15
L14	L13 and context	116	L14
L13	L12 near20 pipelin$4	242	L13
L12	(halt$3 or hold$3 or held or inhibit$3) near14 (stall$3 or priorit$7)	9526	L12
L11	l7 not l8	18	L11
L10	L8 not l9	5	L10
L9	L8 and priorit$8	16	L9
L8	L7 and stall$3	21	L8
L7	L4 and context	39	L7
DB=PGPB,USPT; PLUR=YES; OP=OR			
L6	L4 and context	38	L6
L5	(712/2-300)[CCLS]	9790	L5
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	(halt$3 or hold$3 or held or inhibit$3 or suspend$3) near8 (detect$3 or determin$7) near15 pipelin$7	278	L4
L3	(halt$3 or inhibit$3 or suspend$3) near8 (detect$3 or determin$7) near15 pipelin$7 near7 fetch$3	1	L3
L2	(halt$3 or inhibit$3 or suspend$3) near8 (detect$3 or determin$7) near15 pipelin$6 near15 (second or next or subsequent$2)	8	L2
L1	(halt$3 or inhibit$3 or suspend$3) near6 (detect$3 or determin$7) near15 pipelin$6 near5 (second or next or subsequent$2)	5	L1

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 21 through 40 of 40 returned.

☐ 21. Document ID: US 5842031 A

Using default format because multiple data bases are involved.

L6: Entry 21 of 40 File: USPT Nov 24, 1998

US-PAT-NO: 5842031
DOCUMENT-IDENTIFIER: US 5842031 A

TITLE: Advanced parallel array processor (APAP)

DATE-ISSUED: November 24, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Barker; Thomas Norman	Vestal	NY		
Collins; Clive Allan	Poughkeepsie	NY		
Dapp; Michael Charles	Endwell	NY		
Dieffenderfer; James Warren	Owego	NY		
Grice; Donald George	Kingston	NY		
Kogge; Peter Michael	Endicott	NY		
Kuchinski; David Christoper	Owego	NY		
Knowles; Billy Jack	Kingston	NY		
Lesmeister; Donald Michael	Vestal	NY		
Miles; Richard Ernest	Apalachin	NY		
Nier; Richard Edward	Apalachin	NY		
Retter; Eric Eugene	Warren Center	PA		
Richardson; Robert Reist	Vestal	NY		
Rolfe; David Bruce	West Hurley	NY		
Schoonover; Nicholas Jerome	Tioga Center	NY		
Smoral; Vincent John	Endwell	NY		
Stupp; James Robert	Endwell	NY		
Wilkinson; Paul Amba	Apalachin	NY		

US-CL-CURRENT: 712/23

Full | Title | Citation | Front | Review | Classification | Date | Reference | [illegible] | [illegible] | Claims | KWIC | Draw De

☐ 22. Document ID: US 5794059 A

h e b b cg b cc e

L6: Entry 22 of 40 File: USPT Aug 11, 1998

US-PAT-NO: 5794059
DOCUMENT-IDENTIFIER: US 5794059 A
** See image for Certificate of Correction **

TITLE: N-dimensional modified hypercube

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 23. Document ID: US 5765011 A

L6: Entry 23 of 40 File: USPT Jun 9, 1998

US-PAT-NO: 5765011
DOCUMENT-IDENTIFIER: US 5765011 A

TITLE: Parallel processing system having a synchronous SIMD processing with processing elements emulating SIMD operation using individual instruction streams

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 24. Document ID: US 5761523 A

L6: Entry 24 of 40 File: USPT Jun 2, 1998

US-PAT-NO: 5761523
DOCUMENT-IDENTIFIER: US 5761523 A

TITLE: Parallel processing system having asynchronous SIMD processing and data parallel coding

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 25. Document ID: US 5754871 A

L6: Entry 25 of 40 File: USPT May 19, 1998

US-PAT-NO: 5754871
DOCUMENT-IDENTIFIER: US 5754871 A

TITLE: Parallel processing system having asynchronous SIMD processing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 26. Document ID: US 5752071 A

L6: Entry 26 of 40 File: USPT May 12, 1998

h e b b cg b cc e

US-PAT-NO: 5752071
DOCUMENT-IDENTIFIER: US 5752071 A

TITLE: Function coprocessor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 27. Document ID: US 5752067 A

L6: Entry 27 of 40 File: USPT May 12, 1998

US-PAT-NO: 5752067
DOCUMENT-IDENTIFIER: US 5752067 A

TITLE: Fully scalable parallel processing system having asynchronous SIMD processing

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 28. Document ID: US 5734921 A

L6: Entry 28 of 40 File: USPT Mar 31, 1998

US-PAT-NO: 5734921
DOCUMENT-IDENTIFIER: US 5734921 A
** See image for Certificate of Correction **

TITLE: Advanced parallel array processor computer package

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 29. Document ID: US 5717944 A

L6: Entry 29 of 40 File: USPT Feb 10, 1998

US-PAT-NO: 5717944
DOCUMENT-IDENTIFIER: US 5717944 A

TITLE: Autonomous SIMD/MIMD processor memory elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 30. Document ID: US 5717943 A

L6: Entry 30 of 40 File: USPT Feb 10, 1998

US-PAT-NO: 5717943
DOCUMENT-IDENTIFIER: US 5717943 A

TITLE: Advanced parallel array processor (APAP)

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 31. Document ID: US 5713037 A

L6: Entry 31 of 40 File: USPT Jan 27, 1998

US-PAT-NO: 5713037
DOCUMENT-IDENTIFIER: US 5713037 A
** See image for Certificate of Correction **

TITLE: Slide bus communication functions for SIMD/MIMD array processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 32. Document ID: US 5710935 A

L6: Entry 32 of 40 File: USPT Jan 20, 1998

US-PAT-NO: 5710935
DOCUMENT-IDENTIFIER: US 5710935 A

TITLE: Advanced parallel array processor (APAP)

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 33. Document ID: US 5708836 A

L6: Entry 33 of 40 File: USPT Jan 13, 1998

US-PAT-NO: 5708836
DOCUMENT-IDENTIFIER: US 5708836 A

TITLE: SIMD/MIMD inter-processor communication

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☑ 34. Document ID: US 5590349 A

L6: Entry 34 of 40 File: USPT Dec 31, 1996

US-PAT-NO: 5590349
DOCUMENT-IDENTIFIER: US 5590349 A

TITLE: Real time programmable signal processor architecture

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b cg b cc e

☐ 35. Document ID: US 5590345 A

L6: Entry 35 of 40 File: USPT Dec 31, 1996

US-PAT-NO: 5590345
DOCUMENT-IDENTIFIER: US 5590345 A
** See image for Certificate of Correction **

TITLE: Advanced parallel array processor(APAP)

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☐ 36. Document ID: US 5588152 A

L6: Entry 36 of 40 File: USPT Dec 24, 1996

US-PAT-NO: 5588152
DOCUMENT-IDENTIFIER: US 5588152 A
** See image for Certificate of Correction **

TITLE: Advanced parallel processor including advanced support hardware

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☑ 37. Document ID: US 5581773 A

L6: Entry 37 of 40 File: USPT Dec 3, 1996

US-PAT-NO: 5581773
DOCUMENT-IDENTIFIER: US 5581773 A

TITLE: Massively parallel SIMD processor which selectively transfers individual contiguously disposed serial memory elements

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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☑ 38. Document ID: US 5392448 A

L6: Entry 38 of 40 File: USPT Feb 21, 1995

US-PAT-NO: 5392448
DOCUMENT-IDENTIFIER: US 5392448 A
** See image for Certificate of Correction **

TITLE: Real-time operating system and virtual digital signal processor for the control of a computer

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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h e b b cg b cc e

☐ 39. Document ID: US 5287537 A

L6: Entry 39 of 40 File: USPT Feb 15, 1994

US-PAT-NO: 5287537
DOCUMENT-IDENTIFIER: US 5287537 A

TITLE: Distributed processing system having plural computers each using identical retaining information to identify another computer for executing a received command

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 40. Document ID: US 5187796 A

L6: Entry 40 of 40 File: USPT Feb 16, 1993

US-PAT-NO: 5187796
DOCUMENT-IDENTIFIER: US 5187796 A
**** See image for Certificate of Correction ****

TITLE: Three-dimensional vector co-processor having I, J, and K register files and I, J, and K execution units

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
(5 AND 2).PGPB,USPT.	40
(L5 AND L2).PGPB,USPT.	40

Display Format: - Change Format

Previous Page Next Page Go to Doc#

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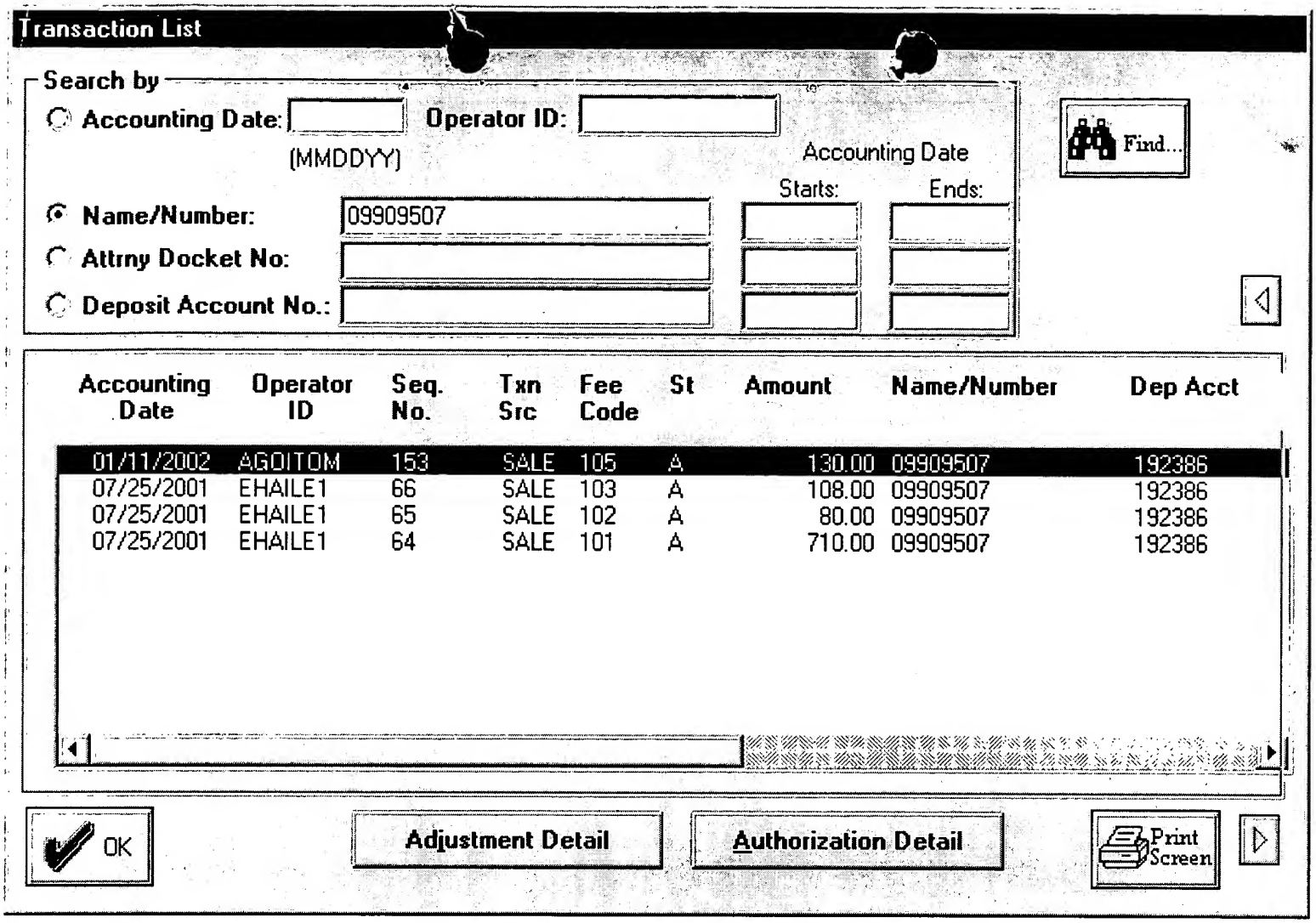
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Amount
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Dep Acct
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07/25/2001 EHAILE1 66 SALE 103 A 108.00 09909507 192386
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